This listing of the claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Currently amended) A multi-layer circuit board, comprising:

at least one signal trace disposed on a dielectric layer, wherein the at least one signal trace comprises a first width that is wider than a second width; ~~and~~

at least one via electrically connected to the first width of the at least one signal trace~~.~~ , wherein an impedance discontinuity between the at least one signal trace and a component electrically connected to the at least one via is lowered from above about 5 ohms to less than about 1 ohm.

2. (Original) The multi-layer circuit board of claim 1 wherein the ratio of the first width to the second width is between about 2:1 and 3:1.

3. (Original) The multi-layer circuit board of claim 1 wherein the first width of at least one signal trace is located in a signal trace anti-pad region, wherein the signal trace anti-pad region extends from the center of the via to slightly past the edge of an anti-pad region.

4. (Original) The multi-layer circuit board of claim 1 wherein the second width of the at least one signal trace is located in a ground plane region, wherein the ground plane region extends from slightly past the edge of an anti-pad region to the end of the signal

trace opposite the first width of the signal trace.

5. (Original) The multi-layer circuit board of claim 1 wherein the signal trace further comprises a via pad.

6. (Original) The multi-layer circuit board of claim 1 wherein the first width of the at least one signal trace is not substantially disposed over a ground plane.

7. (Cancelled)

8. (Currently amended) A test structure, comprising:

at least one signal trace disposed on a dielectric layer, wherein the at least one signal trace comprises a first width that is wider than a second width;

a via connected to the first width of the at least one signal trace; and

a component electrically attached to the via, ~~wherein an impedance discontinuity between the at least one signal trace and the component is lowered.~~ wherein an impedance discontinuity between the at least one signal trace and the component is lowered from above about 5 ohms to below about 1 ohm.

9. (Original) The test structure of claim 8 wherein the ratio of the first width to the second width is between about 2:1 and 3:1.

10. (Original) The test structure of claim 8, wherein the first width is located in a signal trace anti-pad region, and the second width is located in a ground plane region.

11. (Currently amended) The test structure of claim 8 wherein the at least one signal trace is not substantially disposed over an underlying ground plane in ~~the~~ a signal trace anti-pad region.

12. (Original) The test structure of claim 8 wherein the component is one of a SMA, BNC or SIP connector.

13. (Original) The test structure of claim 8 wherein the component is one of a socket, a microprocessor, or a circuit component.

14. (Cancelled)

15. (Original) The test structure of claim 8, wherein the component is adapted for receiving a signal.

16. (Currently amended) The test structure of claim ~~8~~ 15, wherein the signal is launched through a prober and a signal output is coupled to the component.

17. (Original) The test structure of claim 15, wherein the signal has a frequency of

above about 5 Gigahertz.

18. (Currently amended) A test system, comprising:

a TDR prober including a signal output and a signal ground;

at least one ground pad disposed on a dielectric layer, wherein the ground pad is coupled to the signal ground;

at least one signal trace disposed on the dielectric layer, wherein the at least one signal trace comprises a first width that is wider than a second width; and

a component electrically connected to the first width of the at least one signal trace, ~~and~~ wherein the component is coupled to the signal output. and wherein an impedance discontinuity between the at least one signal trace and the component is lowered from above about 5 ohms to less than about 1 ohm.

19. (Original) The test system of claim 18 wherein the ratio of the first width to the second width is between about 2:1 and 3:1.

20. (Original) The test system of claim 18 wherein the component is a SMA connector.

21. (Original) The test system of claim 18 wherein the TDR prober comprises a TDR probing system.

22. (Cancelled)

23. (Currently amended) A method of forming a test structure, comprising:

forming a signal trace on a dielectric layer, wherein the signal trace comprises a first width that is wider than a second width;

electrically connecting a via to the first width of the signal trace; and

electrically connecting a component to the via, ~~wherein the impedance discontinuity between the signal trace and the component is lowered.~~ wherein an impedance continuity between the signal trace and the component is lowered from above about 5 ohms to below about 1 ohm.

24. (Original) The method of claim 23 wherein forming the signal trace comprises forming the first width of the signal trace to be wider than the second width by a ratio of between about 2:1 to about 3:1.

25. (Cancelled)